| 招生學年度 | 103 | 招生類別 | 碩士班 |
|---|---|---|---|
| 系所班別 | 電機光電碩士班聯合招生（電機工程學系碩士班、電機工程學系 電子工程碩士班、光電工程學系碩士班） | | |
| 科目名稱 | 電子學 | | |
| 注意事項 | 本考科可使用掌上型計算機 | | |

1. A Si pn junction employs $N_A = 10^{16}$ cm$^{-3}$ and $N_D = 2\times10^{15}$ cm$^{-3}$. (a) Estimate the minority carrier concentrations on both sides at room temperature. (b) Sketch the electric filed and potential in the pn junction with a reverse bias voltage $V_R = 2$ V. (10%)
2. For the circuit shown in Fig. 1, assume the common-emitter current gain of the BJT is 100, and neglect the Early effect. Find $R_{in}$ and $v_o/v_{sig}$. (12%)

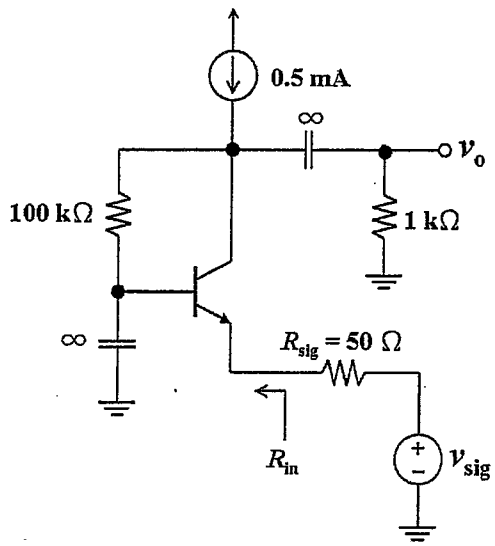


Fig. 1

3. Draw a cross section of a CMOS inverter. Clearly indicate source, drain, gate, oxide, n-type and p-type regions, and input and output terminals. (10%)
4. Fig. 2 shows a MOS amplifier with $V_t = 0.5$ V and $k_n'(W/L) = 2$ mA/V$^2$. Neglect the channel length modulation effect. (a) Find dc values of $V_{GS}$, $I_D$, and $V_D$. (b) Find $g_m$, $R_{in}$, $R_{out}$, and $v_o/v_{sig}$. (18%)

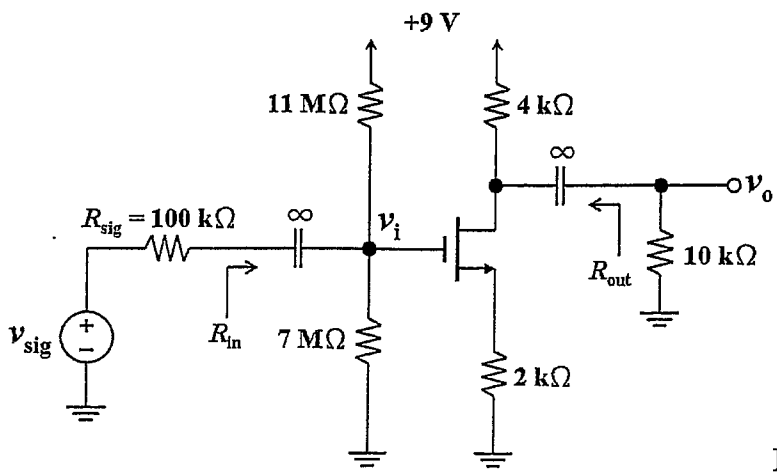


Fig. 2

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5. The PMOS cascode of Fig. 3 is designed for a given output impedance $R_{out}$. Explain what happens to $R_{out}$ if the widths of all transistors are increased by a factor of N while the transistor lengths and bias currents remain unchanged. Assume channel-length modulation parameter $\lambda$ is inversely proportional to channel length. Also assume all transistors operate in saturation and $g_m r_o >> 1$. (15%)

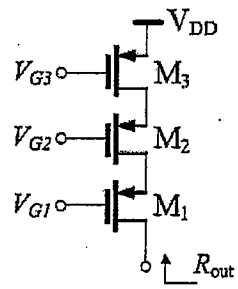


Fig. 3

6. (a) If a resistance has appeared in series with the source of MOSFET as shown in Fig. 4(a), determine the input and output poles of the circuit. Assuming $\lambda = 0$, and neglecting other capacitances except for $C_{in}$ and $C_L$. (b) Repeat (a) for the circuit shown in Fig. 4(b). (20%)

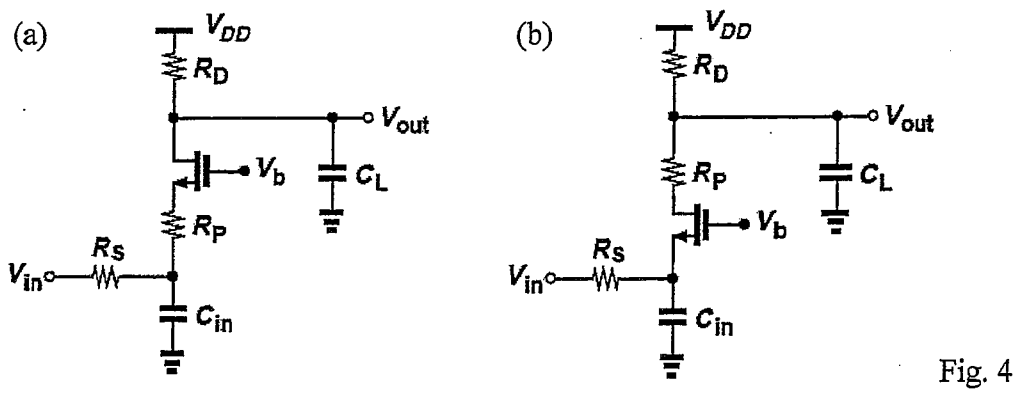


Fig. 4

7. Compute the input impedance $R_{in}$ and output impedance $R_{out}$ of the circuit shown in Fig. 5. Assume $R_1+R_2 >> R_D$. (15%)

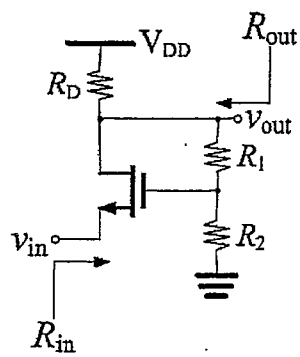


Fig. 5